REMARKS/ARGUMENTS

In this amendment, no claims are amended or canceled. Claim 23 has been added. Thus, after entry of this amendment, claims 1-23 will be pending.

Rejection under 35 U.S.C. § 103, Diamant in view of Benson

Claims 1-6, 13-15, 18, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant (U.S. Patent Publication No. 200410122997) in view of Benson et al. ("Benson") (U.S. Patent No. 5,542,076).

Claims 1-13

Claim 1 is allowable over Diamant and Benson, either alone or in combination, as those references fail to disclose or suggest all the elements of claim 1. For example, claim 1 recites:

> *in response to a detected interrupt, determining whether the detected interrupt was generated by one of the plurality of co-processors of the multiprocessor subsystem; and*
>
> *in the event that the detected interrupt was generated by one of the plurality of co-processors, scheduling execution of a deferred servicing procedure,*
>
> *wherein during execution the deferred servicing procedure services a plurality of pending interrupts generated by two or more of the plurality of co-processors, including the detected interrupt.*

Benson is directed to processing interrupts that occur frequently, but not continuously. *See Benson*, col. 3 lines 1-15. An event detector 50 sends an interrupt to controller 30. *Id.*, col. 4 lines 53-55. Initially, the interrupt flag register 66 has an enabled state so controller 30 services, i.e. does not ignore, the initial interrupt. *Id.*, col. 4 lines 60-67. When processor 70 receives the interrupt signal, it changes the contents of register 66 to represent the disabled state. *Id.*, col. 5 lines 7-10. Once the interrupt routine is completed, register 66 is reset to enabled so that processor 70 may respond to further interrupt signals. *Id.*, col. 5 lines 23-27. The state of processor 70 is then restored by retrieving pre-interrupt values of program counter 90. *Id.*, col. 5 lines 27-33. In addition, the interrupt counter 160 is incremented by one. *Id.*, col. 5 lines 34-35. Thus, only one interrupt is serviced during execution of the interrupt process. In

contrast, claim 1 recites that during execution the servicing procedure services a plurality of pending interrupts generated by two or more co-processors.

In Benson, even when groups of interrupts are received, separate servicing procedures are performed for each interrupt. For example, the prior art handled the interrupt group 270 of FIG. 2 in the following manner. After the processing of each interrupt is complete, the contents of interrupt counter 160 is compared with a threshold value THLD. *Id.*, col. 5 lines 60-64. If the value is exceeded, the interrupt service is disabled for a time Toff. *Id.*, col. 6 line 1-4. The additional check of comparing the THLD with the interrupt counter 160 does not change that servicing of each interrupt is completed and then a new servicing procedure handles the next interrupt, as described at col. 5 lines 1-35.

This separate handling of interrupts is further clarified by Benson's solution to the problem of interrupts that occur frequently, but not continuously. *Id.*, col. 6 lines 5-14. Fig 5 outlines the process for handling the interrupts, whether occurring singly or consecutively as mentioned in col. 6 lines 5-14 of Benson.

At the beginning of each time period T, interrupt servicing is enabled. *Id.*, col. 6 lines 25-26. Once an interrupt is received, interrupts are disabled in step 300, the received interrupt is serviced at step 320 in the known manner (i.e. as described above), the interrupts are reenabled (33), and the value CNT in interrupt counter 160 is incremented. *Id.*, col. 6 lines 33-43. If CNT becomes greater than the threshold value THLD in the threshold register 180, then servicing interrupts is disabled for the rest of the period T so that controller 30 can do other work. *Id.*, col.6 lines 46-57. Thus, again each interrupt is serviced by a separate interrupt process.

As to Diamant, the Office Action states that "Diamant does not expressly teach wherein the system services a plurality of interrupts generated by two or more of the plurality of co-processors." *See Office Action*, page 4 lines 4-5. In Diamant, there is one device driver 18 for each device 10. *See Diamant*, paragraph 21. ("The operating system 12 further loads into memory 6 and executes one device driver 18… for each device 10… recognized by the operating system 12.") (emphasis added).

Thus, neither Diamant nor Benson teach or suggest that a servicing procedure, scheduled in response to a detected interrupt, "services a plurality of pending interrupts generated by two or more of the plurality of co-processors," as recited by claim 1. For at least these reasons, claim 1 is allowable over Diamant in view of Simpson. As claim 1 is allowable, dependent claims 2-13 and 22-23 are also allowable for at least the same rationale.

Claims 14-21

Applicant submits that independent claims 14 and 21 should be allowable for at least the same reasons as claim 1. Claims 15-20 depend from claim 14, and thus derive patentability at least therefrom.

Rejection under 35 USC § 103,

Claims 10-12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant in view of Benson as applied to claim 1 above (hereinafter "Diamant- Benson"), and further in view of Simpson (U.S. Patent No. 5,867,687). As noted on page 12 of the present Office Action, Simpson does not have the limitation of claim 1 as argued above. Thus, claims 10-12, which depend upon claim 1, and claim 17, which depends upon claim 14, are allowable for at least the same rationale as claim 1.

Claims 8, 16, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant-Benson in view of Alasti et al. ("Alasti") (U.S. Patent No. 6,574,693). Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant- Benson in view of Alasti as applied to claim 8 above (hereinafter "DBA), and further in view of Simpson.

Claims 8 and 9 depend upon claim 1 and are allowable for at least the same rationale as claim 1. Claims 16 and 22 depend upon claim 14 and is allowable for at least the same rationale as claim 14.

Alasti is directed to the disabling of interrupts from certain subsystems, such as power management, when a processor is within a certain context. *See Alasti*, abstract line 8 and page 5 line 63. Even assuming that this aspect of Alasti teaches disabling interrupts from co-processors of a subsystem in the event of a detected interrupt being generated by one of the

co-processors of the subsystem and that there is a motivation to combine with Simpson, Diamant and Benson, this teaching does not make up for the deficiencies in these references with respect to these claims.

Objection to Claims 7 and 20

Claims 7 and 20 were objected to as being dependent on a rejected base claim, but were found to be allowable if rewritten in independent form. In view of the foregoing arguments with regard to claims 1 and 14, Applicant respectfully submits that claims 7 and 20 are in condition for allowance without being rewritten in independent form. Withdrawal of the objection is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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